

High Performance Mono Audio CODEC

FEATURES

System

- High performance and low power multi-bit delta-sigma audio ADC and DAC
- I²S/PCM master or slave serial data port
- 256/384Fs and USB 12/24 MHz audio system clocks
- I²C interface

Mono ADC

- 24-bit, 8 to 96 kHz sampling frequency
- 101 dB signal to noise ratio, -90 dB THD+N
- One pair of analog input with differential input option
- Low noise pre-amplifier
- Support analog and digital microphone

Mono Digital Class D

- 8 to 96 kHz sampling frequency
- 102 dB signal to noise ratio
- 1.25W@4Ω
- Over current and temperature protection
- Pop and click noise suppression

Low Power

- 1.8V to 3.3V operation
- mW playback and record
- Low standby current

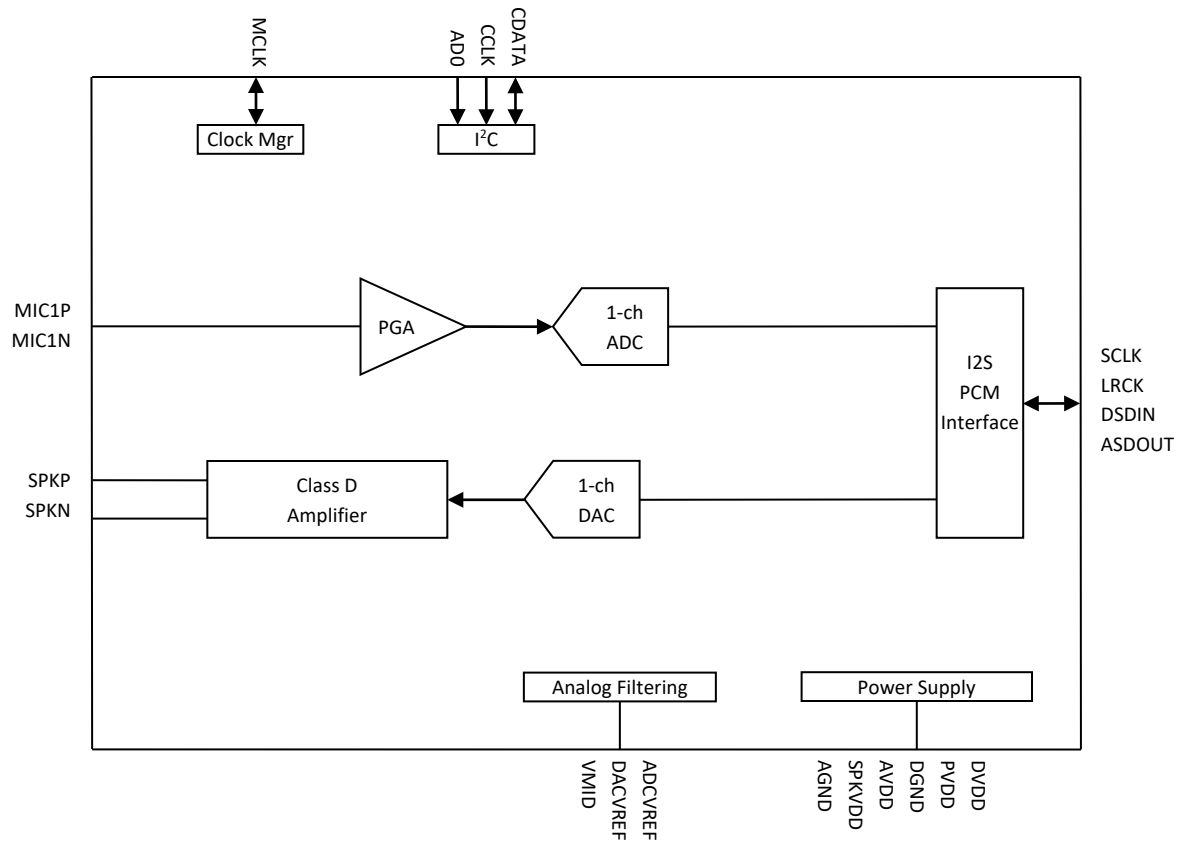
APPLICATIONS

- CAT1
- Camera
- General Purpose

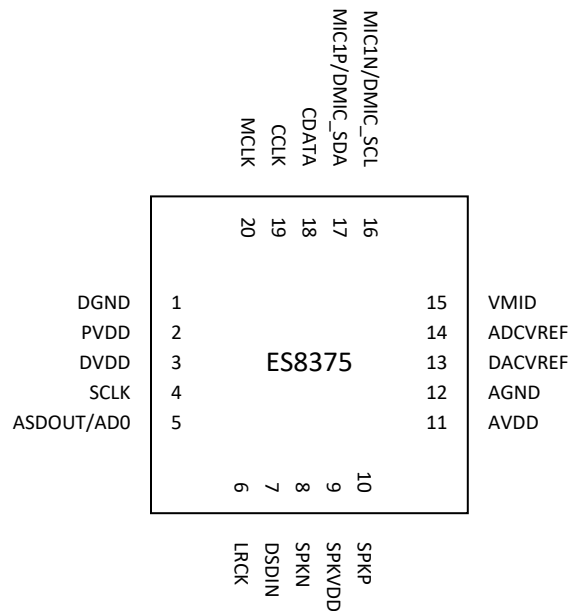
ORDERING INFORMATION

ES8375 -40°C ~ +125°C
3x3 QFN-20

1. BLOCK DIAGRAM

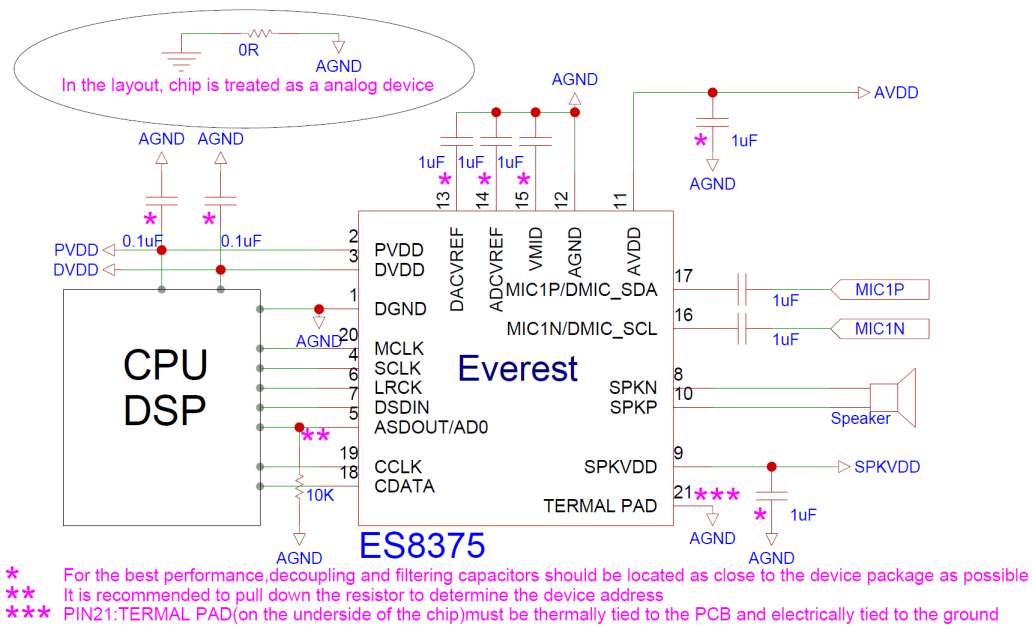


2. PIN OUT AND DESCRIPTION



Pin Name	Pin number	Input or Output	Pin Description
CCLK, CDATA	19, 18	I, I/O	I ² C clock, data
MCLK	20	I	Master clock
SCLK	4	I/O	Serial data bit clock
LRCK	6	I/O	Serial data left and right channel frame clock
ASDOUT/AD0	5	O/I	ADC serial data output/ I ² C address
DSDIN	7	I	DAC serial data input
MIC1P/DMIC_SDA MIC1N/DMIC_SCL	17 16	Analog/I Analog/O	Mic/line input or DMIC data and clock
SPKP, SPKN	10, 8	O	Mono speaker output
DVDD, PVDD, DGND	3, 2, 1	Analog	Digital power supply, PVDD for digital I/O
AVDD, AGND	11, 12	Analog	Analog power supply
SPKVDD	9	Analog	Speaker power supply
VMID	15	Analog	Filtering capacitor connection
ADCVREF, DACVREF	14, 13	Analog	Filtering capacitor connection
THERMAL PAD	21	Analog	Package bottom plate ground

3. TYPICAL APPLICATION CIRCUIT



4. CLOCK MODES AND SAMPLING FREQUENCIES

The device supports standard audio clocks (32Fs, 64Fs, 128Fs, 256Fs, 384Fs, 512Fs, etc.) and USB clocks (12/24 MHz).

The device can work either in master clock mode or slave clock mode. In slave mode, LRCK and SCLK are supplied externally, and LRCK and SCLK must be synchronously derived from the system clock with specific rates. In master mode, LRCK and SCLK are derived internally from device master clock.

5. MICRO-CONTROLLER CONFIGURATION INTERFACE

The device supports standard I²C micro-controller configuration interface. External micro-controller can completely configure the device through writing to internal configuration registers.

I²C interface is a bi-directional serial bus that uses a serial data line (CDATA) and a serial clock line (CCLK) for data transfer. The timing diagram for data transfer of this interface is given in Figure 1a and Figure 1b. Data are transmitted synchronously to CCLK clock on the CDATA line on a byte-by-byte basis. Each bit in a byte is sampled during CCLK high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the CDATA low. The transfer rate of this interface can be up to 400 kbps.

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at CDATA while CCLK is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The chip address must be 001100x, where x equals AD0 (input pin: 1 being digital input high and 0 being digital input low). The RW bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at CDATA while CCLK is high.

In I²C interface mode, the registers can be written and read. The formats of “write” and “read” instructions are shown in Table 1 and Table 2. Please note that, to read data from a register, you must set R/W bit to 0 to access the register address and then set R/W to 1 to read data from the register.

Table 1 Write Data to Register in I²C Interface Mode

	Chip Address	R/W		Register Address		Data to be written		
start	001100 AD0	0	ACK	RAM	ACK	DATA	ACK	Stop

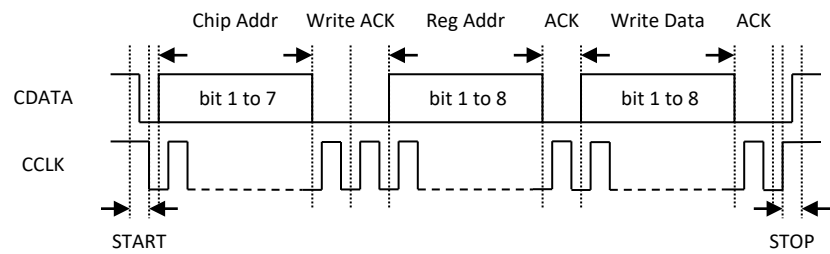


Figure 1a I²C Write Timing

Table 2 Read Data from Register in I²C Interface Mode

	Chip Address	R/W		Register Address		
Start	001100 AD0	0	ACK	RAM	ACK	
	Chip Address	R/W		Data to be read		
Start	001100 AD0	1	ACK	Data	NACK	Stop

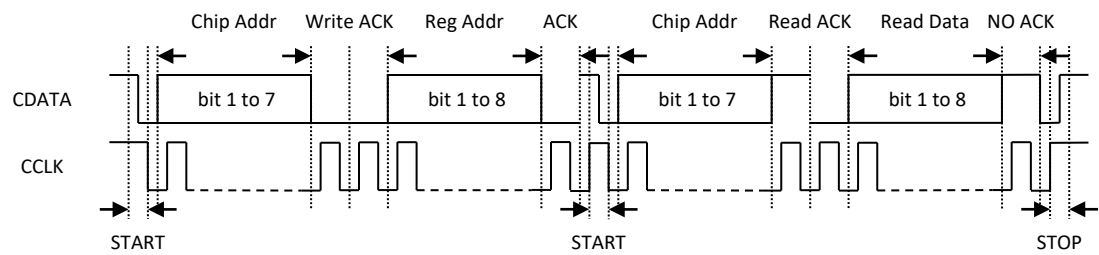


Figure 1b I²C Read Timing

6. I²S/PCM INTERFACE

The device provides many formats of serial audio data interface to the input of the DAC or output from the ADC through LRCK, SCLK and SDIN or SDOUT pins. These formats are I²S, left justified and DSP/PCM. DAC input SDIN is sampled by the device on the rising edge of SCLK. ADC data is out at SDOUT on the falling edge of SCLK. The relationship of SDATA (SDIN/SDOUT), SCLK and LRCK with these formats are shown through Figure 2a to Figure 2d.

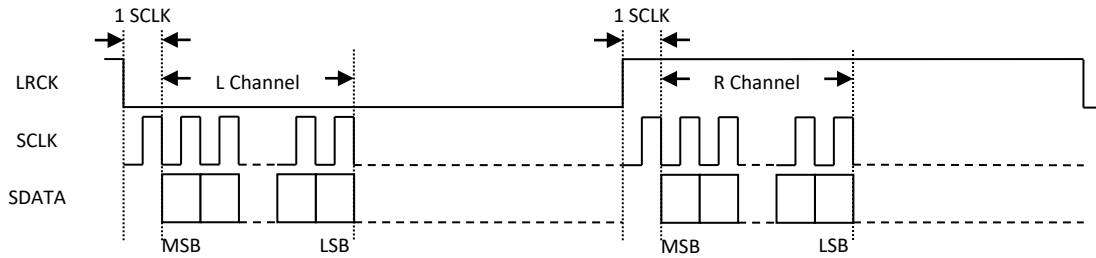


Figure 2a I²S Serial Audio Data Format

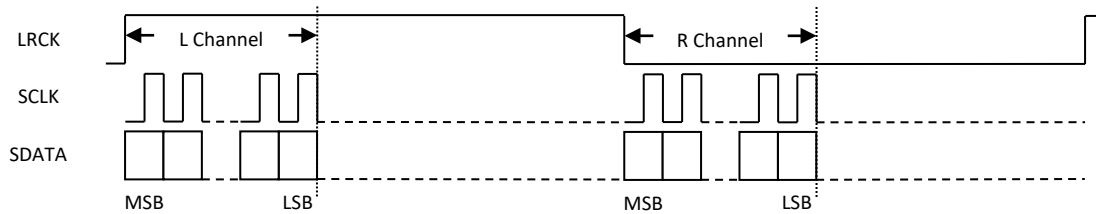


Figure 2b Left Justified Serial Audio Data Format

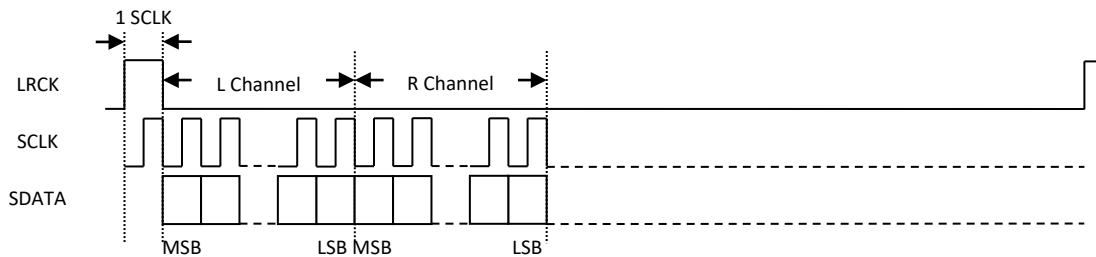


Figure 2c DSP/PCM Mode A Serial Audio Data Format

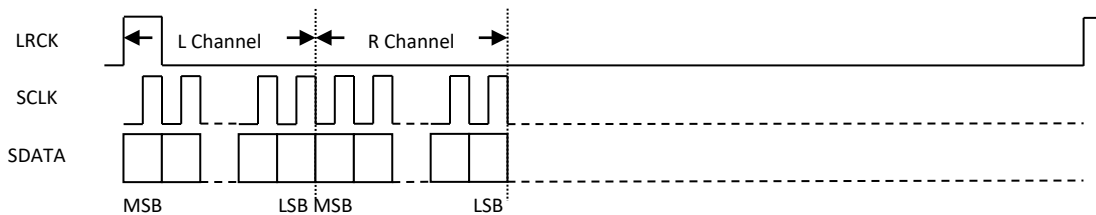


Figure 2d DSP/PCM Mode B Serial Audio Data Format

7. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Analog Input Voltage Range	AGND-0.3V	AVDD+0.3V
Digital Input Voltage Range	DGND-0.3V	PVDD+0.3V
Operating Temperature Range	-40°C	+125°C
Storage Temperature	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
DVDD	1.6	1.8/3.3	3.6	V
PVDD (digital I/O voltage)	1.6	1.8/3.3	3.6	V
AVDD	3.0	3.3	3.6	V
SPKVDD	3.0	3.3	3.6	V

ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DVDD=1.8V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
ADC Performance				
Signal to Noise ratio (A-weight)	97	101	103	dB
THD+N	-93	-90	-87	dB
Interchannel Gain Mismatch		0.1	0.5	dB
Gain Error			±5	%
Filter Frequency Response				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	70			dB
Analog Input				
Full Scale Input (differential P and N)		2.2*AVDD/3.3		Vrms
Input Impedance		16		KΩ

DC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
DVDD=1.8V, AVDD=3.3V		49		mW
Power Down Mode (Note 1)				
DVDD=1.8V, AVDD=3.3V		0		uA
Digital Voltage Level				
Input High-level Voltage	0.7*PVDD			V
Input Low-level Voltage			0.5	V
Output High-level Voltage		PVDD		V
Output Low-level Voltage		0		V

Note 1: recommend all power supply on, entering low power through control register setting, then stopping input clock.

SERIAL AUDIO PORT SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
MCLK frequency			49.2	MHz
MCLK duty cycle		40	60	%
LRCK frequency			96	KHz
LRCK duty cycle (Note 2)		40	60	%
SCLK frequency	VDDD=1.8V VDDD=3.3V		13 26	MHz
SCLK pulse width low	T_{SCLKL}	16		ns
SCLK Pulse width high	T_{SCLKH}	16		ns
SCLK falling to LRCK edge (master mode only)	T_{SLR}		5	ns
LRCK edge to SCLK rising (slave mode only)	T_{LSR}	10		ns
SCLK falling to ASDOUT valid	VDDD=1.8V VDDD=3.3V		31.5 12	ns
LRCK edge to ASDOUT valid (Note 3)	VDDD=1.8V VDDD=3.3V		26 10	ns
DSDIN valid to SCLK rising setup time	T_{SDIS}	10		ns
SCLK rising to DSDIN setup time	T_{SDIH}	10		ns

Note 2: one SCLK period of high time in DSP/PCM modes.

Note 3: only apply to MSB of Left Justified or DSP/PCM mode B.

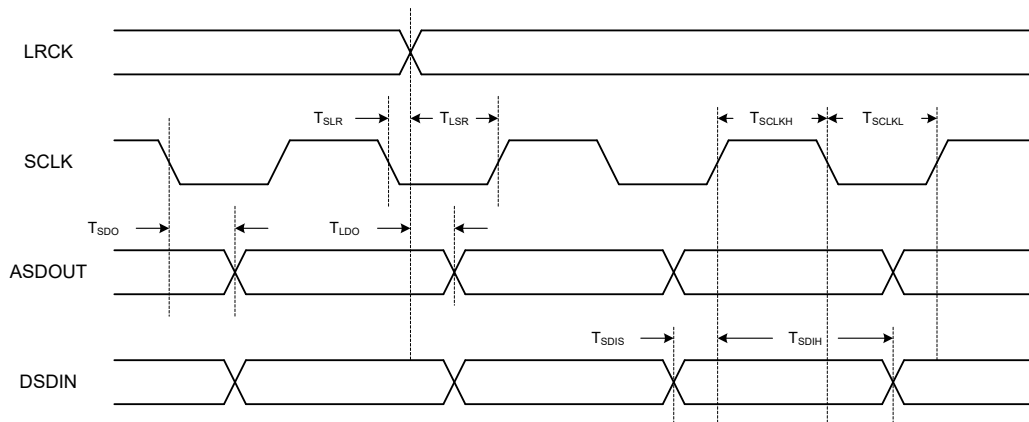
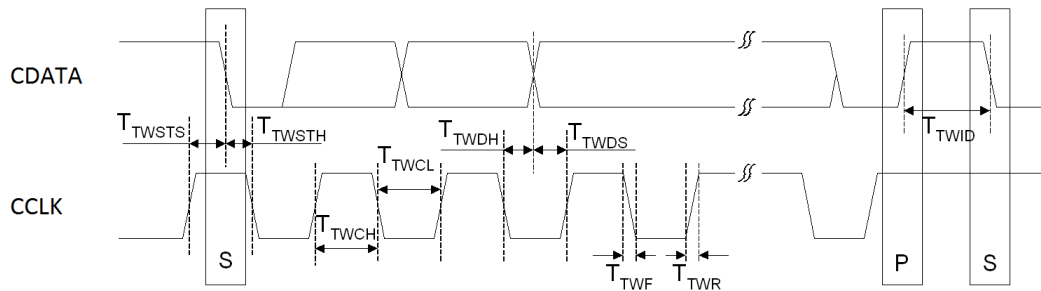


Figure 3 Serial Audio Port Timing

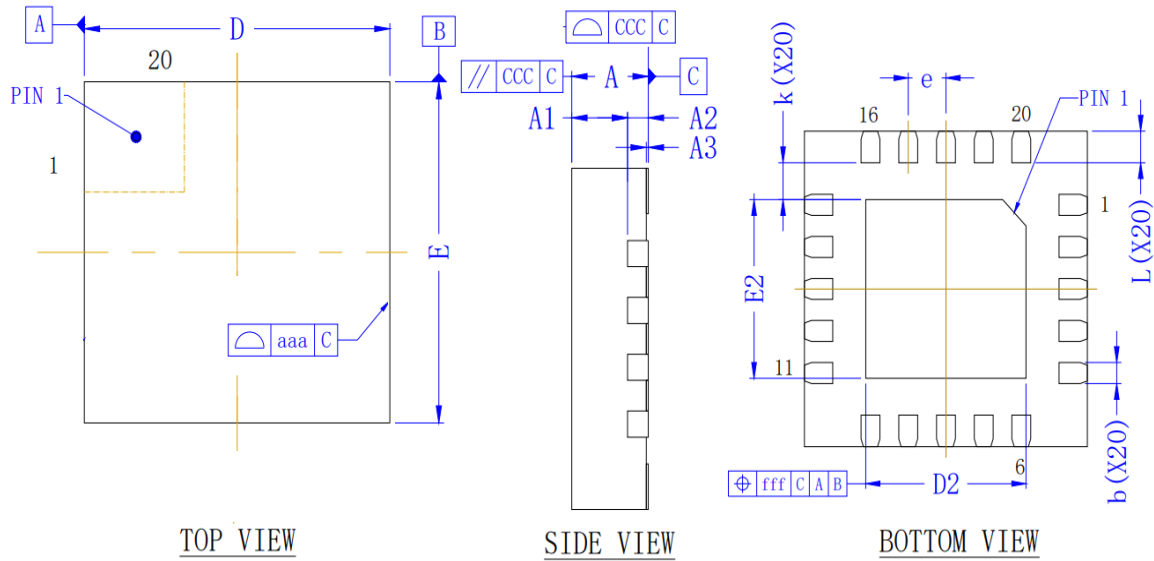
I²C SWITCHING SPECIFICATIONS (SLOW SPEED MODE/HIGH SPEED MODE)

PARAMETER	Symbol	MIN	MAX	UNIT
CCLK Clock Frequency	F _{CCLK}		100/400	KHz
Bus Free Time Between Transmissions	T _{TWID}	4.7/1.3		us
Start Condition Hold Time	T _{TWSTH}	4.0/0.6		us
Clock Low time	T _{TWCL}	4.7/1.3		us
Clock High Time	T _{TWCH}	4.0/0.6		us
Setup Time for Repeated Start Condition	T _{TWSTS}	4.7/0.6		us
CDATA Hold Time from CCLK Falling	T _{TWDH}		3.45/0.9	us
CDATA Setup time to CCLK Rising	T _{TWDS}	0.25/0.1		us
Rise Time of CCLK	T _{TWR}		1.0/0.3	us
Fall Time CCLK	T _{TWF}		1.0/0.3	us

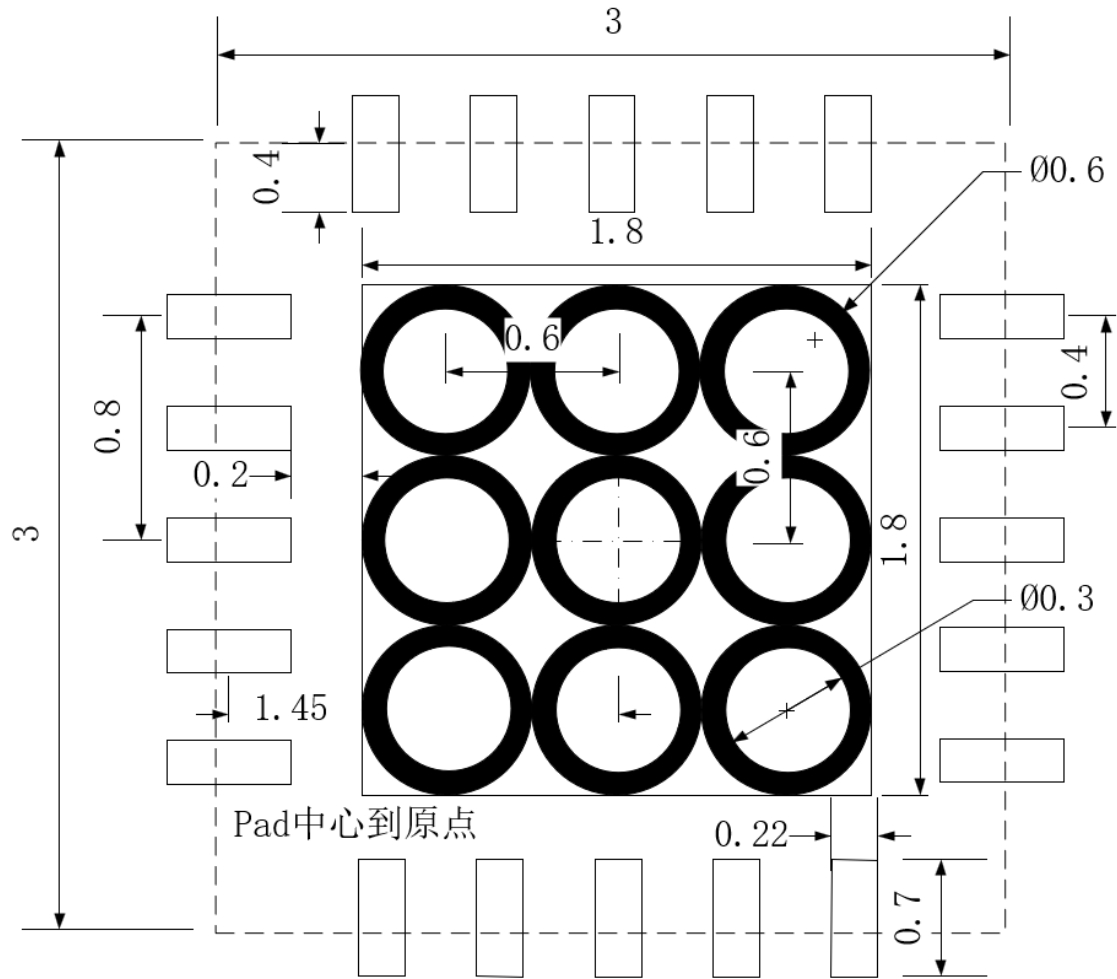
Figure 4 I²C Timing

8. PACKAGE (UNIT: MM)

QFN-20L-3X3(P0.4T0.55) Package Outline Drawing



Item	Symbol	Minimum	Normal	Maximum
Total Thickness	A	0.50	0.55	0.60
Stand Off	A1	0.00	0.02	0.05
Molding Thickness	A2	---	0.40	---
LF Thickness	A3	0.152 REF		
Lead Width	b	0.15	0.20	0.25
Body Size	D	3 BSC		
	E	3 BSC		
Lead Pitch	e	0.4 BSC		
Exposed Pad Size	D2	1.60	1.70	1.80
	E2	1.60	1.70	1.80
Lead Length	L	0.20	0.30	0.40
Lead tip to Exposed Pad	K	0.35 REF		
Package Edge Tolerance	aaa	0.1		
Molding Flatness	ccc	0.1		
Coplanarity	eee	0.08		
Lead Offset	bbb	0.1		
Exposed Pad Offset	fff	0.1		



9. CORPORATE INFORMATION

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